Optimize the Buffer Amplifier/ADC Connection

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> With increasing portions of today's receivers implemented digitally, the conversion of analog signals to the digital domain has become very important for best system performance

Communications systems designers have long envisioned the "ideal" digital receiver signal-processing chain as consisting of an antenna, filter, low-noise amplifier (LNA), and analog-to-digital converter (ADC) followed by digital demodulation and signal processing circuitry. Although this ideal digital receiver may still be several years away, communications receivers have steadily eliminated stages of frequency conversion while placing greater importance on the ADC in the front-end architecture. Although some receiver stages have been eliminated, the buffer amplifier stage that precedes the ADC remains an important component in a wide range of receivers and can play a major role in the performance achieved by the ADC.

The buffer amplifier that's added to the signal processing chain becomes part of a group of functional blocks, including mixers, filters, and other amplifiers, that must be treated as a single component, with a noise figure, gain and intercept point. The proper choice of a buffer amplifier for a given ADC can increase the sensitivity of the receiver without sacrificing the overall spurious-free dynamic range (SFDR).

Defining Dynamic Range

Receiver sensitivity is one component of the system's dynamic range, with sensitivity defining the minimum signal level that allows the receiver to successfully recover the transmitted information. The upper end of the dynamic range is the maximum signal that can be processed. It is usually defined by the third-order intercept point (IP3), an imaginary number that marks the point at which a receiver's front-end components will be overloaded or saturated into compression. Dynamic range is a compromise, of course, because high sensitivity requires a low noise figure and a high gain. Unfortunately, practical LNAs with gains of 30 dB or more and noise figures of less than 2 dB have limited third-order-intercept performance, often with values of +10 to +15 dBm. Thus, these amplifiers can increase receiver sensitivity, but become a "bottleneck" for high-level signals in the receiver's front-end signal-processing chain.

Adding an ADC to the receiver front-end causes the tradeoff for dynamic range to become even more complicated. But newer linear amplifiers with digital control, often referred to as buffer amplifiers, can help to improve overall receiver performance as well as expand dynamic range.

To understand how a buffer amplifier is used with a high-speed ADC, it may help to review the basic performance parameters for each component and how they impact receiver performance. Traditional receiver front ends have employed several stages of frequency conversion to translate high-frequency signals from an antenna to lower IF signals that can be demodulated and further processed. Typical signal chains might translate RF input signals to a first IF of 70 or 140 MHz, a second IF of 10 MHz, and a third IF of 455 kHz. Although this multiple-conversion super-heterodyne receiver approach is still widespread, the cost and size constraints of modern communications systems have pressured designers into eliminating as many frequency-conversion stages as

possible. Military designers have long sought the true "all-digital" receiver with an ADC capable of digitizing signals directly from an antenna and filter bank.

ADC performance levels have improved dramatically over the last several years, but not to the point of supporting the all-digital military receiver. Still, commercial receiver designs have been pared from three or more frequency-conversion stages to a single-stage architecture. Fewer frequency-conversion stages, however, result in a relatively high IF at the input of the ADC, requiring a converter and buffer amplifier with generous bandwidth.

The required bit resolution of the ADC depends on the receiver application. For some military applications, such as activity receivers, 10-bit quantization provides adequate resolution. For current and emerging commercial communications receivers, such as 3G and 4G cellular systems, better resolution is needed to minimize quantization errors on waveforms with complex, phase- and amplitude-based modulation formats. Typically 14-bit or higher resolution is needed for multi-carrier receivers, along with sufficient bandwidth to accept the full IF band.

Assuming that a high-speed, high-resolution ADC is available for a given receiver IF architecture, what are the other key performance parameters that will have a bearing on sensitivity and dynamic range? ADCs are characterized in terms of their spurious-free dynamic range (SFDR), which describes the ratio of the amplitude of the fundamental-frequency input signal to the root-mean-square (RMS) value of the largest distortion component in a specified frequency spectrum. When the input voltage amplitude rises above the maximum allowed range, the sampled output waveform becomes clipped and distorted. Below the minimum recommended input level, all of the ADC's bits may not be

used to represent the waveform, and a 14-bit ADC may essentially perform as a 10- or 12-bit component.

The maximum input voltage (V_{max}) of a sine wave for a given ADC can be found from [1]

$$2V_{max} = 2^b Q \text{ or } V_{max} = 2^{b-1} Q$$

where b is the number of bits for the ADC and Q is the voltage per quantization level.

The maximum power level of a sine wave matching the maximum voltage is [1]

$$P_{max} = V^2_{max} / 2 = [2^{2(b-1)}Q^2] / 2$$

$$= 2^{2b}Q^2 / 8$$

The minimum voltage is the amplitude required to impact 1 LSB, and is calculated as follows:

$$2V_{min} = Q$$

with a corresponding power level of

$$P_{min} = V^2_{min} / 2 = Q^2 / 8$$

The dynamic range (DR) is simply derived from

$$DR = P_{max} / P_{min} = 2^{2b}$$

or in logarithmic format

$$DR = 20\log(P_{max} / P_{min})$$

$$= 20b\log(2)$$

$$= 6b \text{ (in dB units)}$$

or essentially 6 dB per bit.

An ADC's SFDR can be found by using an ADC to measure a full-scale sine wave signal, evaluating the ADC's output with a precision digital-to-analog-converter (DAC) and spectrum analyzer combination, and comparing the level of the fundamental-frequency output to the highest spurious signal. Note that the DAC's dynamic range has to be well above
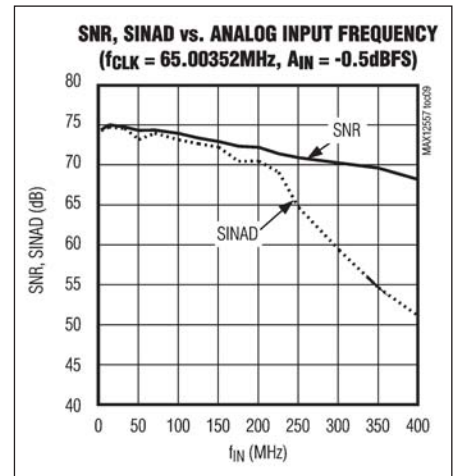

Figure 1 · SNR and SINAD for the 96-MSamples/s MAX12559 ADC, plotted versus input frequency.

that of the ADC to prevent the DAC's dynamic range from becoming the limiting factor while measuring the ADC's SFDR.

High-speed ADCs are currently available with SFDR of better than 80 to 90 dBc. This level is typically measured with either a single tone or two tones at the input of the ADC. For two-tone performance analysis, the two tones could be separated from each other by 1 MHz around the center frequency of a common communications IF, such as 140 MHz. In this case, example tones might be 139.5 and 140.5 MHz.

The sensitivity of a receiver including the ADC is a function of noise level, which itself is a function of bandwidth. Minimize noise and the receiver's sensitivity increases. An ADC's noise floor, which is set by thermal and quantization noise, limits its sensitivity. Quantization noise is essentially the uncertainty associated with the converter's least-significant bit (LSB). In general, an ADC's noise floor is lowest for the lowest-level input signals, increasing as input signal amplitude approaches the converter's FS input value.

As with a receiver, an ADC can be characterized by not only its SFDR performance but also its full-scale-to-

noise ratio and signal-to-noise ratio (SNR). For an ADC, the maximum SNR is a function of its number of bits (*b*):

$$SNR = (1.76 + 6.02b) \text{ dB}$$

An ADC's SNR is essentially the ratio of an RMS full-scale (FS) analog input to the RMS quantization error (Fig. 1). These two components of an ADC's SNR are defined as follows: The RMS value of a sine wave is one-half of its peak-to-peak value divided by the square root of 2. The quantization error is the difference between an analog waveform and its digitally reconstructed replica, with errors occurring due to the uncertainty between –1/2 LSB and +1/2 LSB. By doubling the sampling rate of an ADC, the effective noise figure drops by 3 dB because the noise is being spread across twice the previous bandwidth. The best way to determine an ADC's SNR is by measuring it, using a precision receiver and calibrated noise source. This measurement accounts for clock jitter and other noise sources in the process, and tends to provide realistic, rather than ideal, values for SNR. The SINAD, or signal-to-noise-and-distortion ratio, includes the effects of distortion in the SNR evaluation.

A parameter known as the effective number of bits (ENOB) is used in place of SINAD to indicate an ADC's accuracy for a given input frequency and sampling rate. It is the ratio of a converter's measured and ideal RMS error. The ENOB generally depends on the amplitude and frequency of the applied input sinusoidal signal. The specification compares the RMS noise produced by an ADC to the RMS quantization noise of an ideal ADC under the same conditions and number of bits. For example, a 14-bit ADC with an ENOB of 12-bits produces the same amount of RMS noise as an ideal 12-bit ADC (with a full-scale or near full-scale input signal) under the same input conditions.

$$ENOB = (SINAD - 1.76) / 6.02$$

Total harmonic distortion (THD) is the RMS sum of all harmonics in a signal's FFT spectrum. The first three harmonics represent most of the signal energy. For communications applications, THD is often a more important specification than the DC-linearity specifications that describe static performance. Most manufacturers include harmonics through the fourth or as high as the ninth, referenced to the analog input signal.

As a real-world example of these parameters, consider a commercial ADC from MAXIM Integrated Products, the model MAX12559 (Fig. 2). It consists of two 14-bit ADCs on the same chip, each capable of capturing IF and baseband signals through about 350 MHz at sampling rates to 96 MSamples/s. This dual ADC features internal track-and-hold amplifiers and differential inputs. For a 175-MHz input, it achieves SFDR of 79.8 dBc, with typical SNR of 71.9 dB and SINAD of 70.9 dB (Fig. 3). The THD is –77.9 dBc. The ADC is designed for 3.3 V operation and consumes only 980-mW analog power.

A flexible reference structure allows the device to use the internal 2.048 V bandgap reference or accept an external reference, and allows the reference to be shared between the two ADCs. The reference structure allows the FS analog input range to be adjusted from ±0.35 V to ±1.15 V. The dual ADC can be used with a single-ended or differential clock, and user-selectable divide-by-two and divide-by-four modes simplify the selection of clock sources.

Selecting a Buffer

What kind of buffer amplifier best serves the MAX12559 or similar high-speed ADCs in a modern communications receiver design? Ideally, the buffer should match or exceed the bandwidth of the ADC (750 MHz for
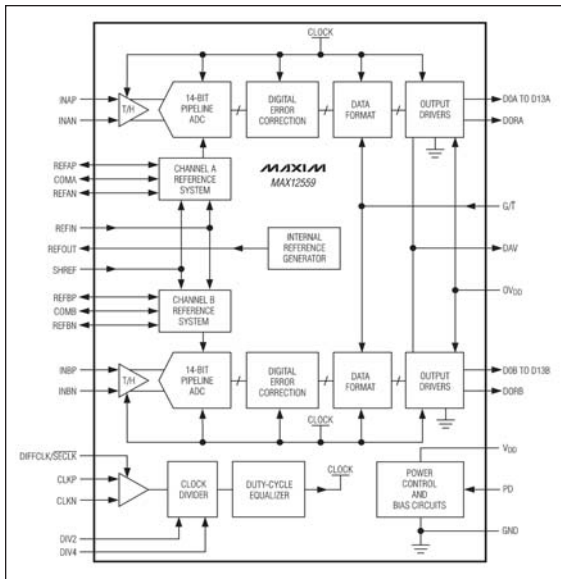
Figure 2 · The MAX12559's two 14-bit ADCs are capable of capturing signals through about 350 MHz at rates to 96 MSamples/s.
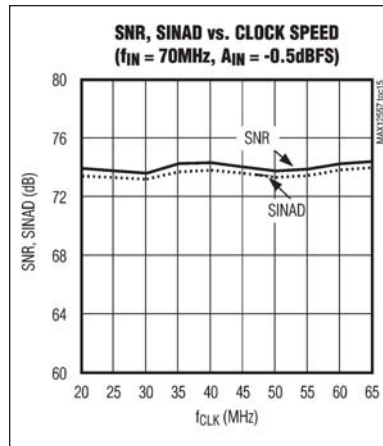

Figure 3 · The SNR and SINAD performance of the MAX12559 ADC remain relatively flat at different clock speeds, with measurements for a 70-MHz input signal at an amplitude level of –1 dBFS.
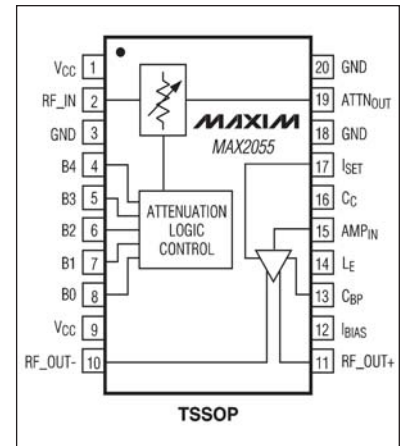

Figure 4 · The MAX2055 buffer amplifier combines a digitally controlled attenuator with a single-ended-to-differential amplifier for flexible interfacing with high-speed ADCs.

the MAX12559), or at least operate within the bandwidth to be sampled, assuming that the full capabilities of the ADC are not needed for a given application. ADC buffer amplifiers are typically specified in terms of frequency-domain characteristics, whereas operational amplifiers are usually specified in terms of settling time and slew rate. Regardless of how the buffer is specified, it must provide the transient response needed for the ADC to receive input waveforms that are not limited or distorted by more than 1 LSB of the ADC.

In a receiver front end, the buffer amplifier's noise figure would contribute, but not dominate. In a cascaded signal processing chain, the first-stage amplifier has the greatest impact on receiver noise figure; normally, the amplifier with the lowest noise figure in the chain is placed first. As a result, the noise figure of a buffer amplifier is not as critical as the noise figure of that first-stage amplifier, although a relatively low buffer-amplifier noise figure will minimize its effect on the overall receiver noise figure. For a buffer amplifier, a noise figure of 6 dB to 7

dB will have minimal effect on a receiver chain with first-stage LNA of 2 dB or lower noise figure.

The buffer amplifier should provide adequate gain to ensure that signals to the ADC approach its FS input voltage level requirement. Perhaps as important, the gain response versus frequency should be tightly controlled; gain flatness should be essentially within an LSB of the ADC. For high-resolution (14 bits or higher) ADCs, this calls for a buffer amplifier with better than ±0.5 dB gain flatness across the bandwidth of interest.

The buffer amplifier should provide good linearity in terms of both output level and intercept-point performance. For example, the amplifier must at least provide an output level compatible with the input requirements of the ADC. Its linearity should ideally exceed that of the ADC to prevent undesired degradation in the ADC's SFDR performance.

Assuming that the spurious contributions of the buffer amplifier and ADC add in phase, the combined SFDR of these two components can be computed as follows:

SFDR System (in dBc) =
$-20\log\{10\exp[(-\text{SFDR ADC}) / 20]$
$+ 10\exp[(-\text{SFDR Buffer}) / 20]\}$

The buffer amplifier should have low enough source impedance to provide isolation from the ADC's input impedance, but enough output power to drive the ADC's inputs. The buffer's high-frequency output impedance must be sufficiently low to avoid excess conversion errors. The buffer amplifier's output impedance will have direct bearing on the ADC's AC performance, especially its THD.

In the case of switched-capacitor ADCs, the converter may draw a small amount of input current at the end of each conversion. When used with this type of converter, a buffer amplifier must be capable of sufficiently fast transient response to avoid conversion errors. Provided the transient response of the buffer is fast enough, which implies a bandwidth of greater than 100 MHz (rise time of 10 ns), errors will be minimal. When the buffer's transient response is inadequate, an RC filter can be added at its output to limit bandwidth according to the requirements
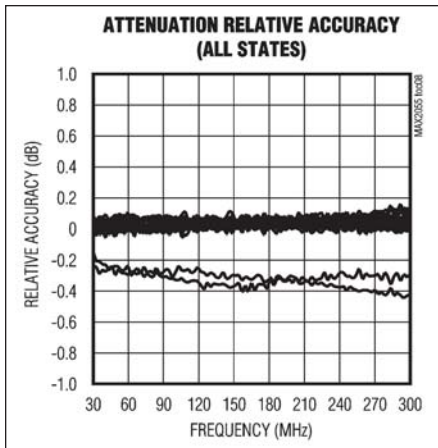
Figure 5 · The MAX2055's built-in attenuator provides precise amplitude control.
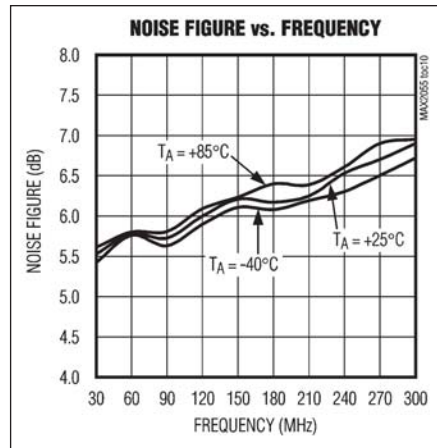

Figure 6 · The MAX2055 buffer amplifier is specified for low noise at its maximum gain setting.
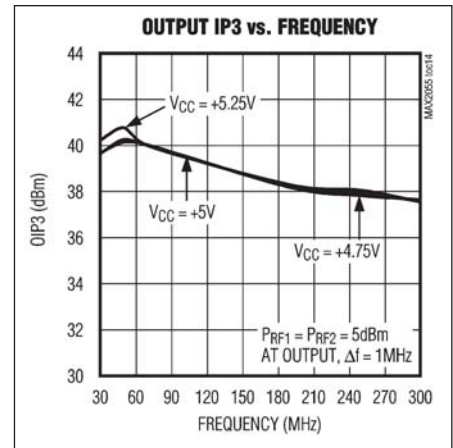

Figure 7 · The MAX2055 achieves a high OIP3 of +40 dBm for all gain settings.

of the receiver, but also to provide extra capacitance to eliminate the ADC transient effect. The filter's capacitance must be larger than the ADC's input capacitance.

Examples of commercially available ADC buffer amplifiers suitable for use with the MAX12559 ADC include models MAX2055 and MAX2027 from MAXIM Integrated Products.

The MAX2055 is a digitally controlled variable-gain amplifier (DVGA) usable with signals from 30 to 300 MHz (Fig. 4). It has a single-ended input and differential output to simplify use with differential ADCs. The buffer amplifier integrates a digitally controlled attenuator and high-linearity amplifier with single-ended-to-differential transformer, eliminating the need for an external single-ended-to-differential transformer or additional amplifier circuit. The built-in attenuator controls a 23-dB range with ±0.2 dB accuracy and can be set dynamically or as a one-time channel gain setting (Fig. 5). It features a 6 dB noise figure at the maximum gain setting (Fig. 6) and output third-order intercept point (OIP3) of +40 dBm for all gain settings (Fig. 7). Maximum output power at the 1-dB compression point is +24 dBm, with –76 dBc for the 2nd-

order harmonic (HD2) and –69 dBc for the 3rd-order harmonic (HD3).

The MAX2027 is also a DVGA, but a single-ended device, with an adjustable gain from –8 dB to +15 dB in 1-dB steps from 50 MHz to 400 MHz. It features a 4.7 dB noise figure at the maximum gain setting, OIP3 of +35 dBm at all gain settings, and impressive ±0.05 dB attenuation accuracy.

References/Further Reading

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4. "How Quantization and Thermal Noise Determine an ADC's Effective Noise Floor," App. Note AN1197, MAXIM Integrated Products, www.maxim-ic.com.

5. "Understanding ADC Noise for Small and Large Signal Inputs for Receiver Applications," App. Note AN1929, MAXIM Integrated Products, www.maxim-ic.com.

6. "Dynamic Performance Requirements for High-Performance ADCs and RF Components in Digital Receiver Applications," App. Note AN3062, MAXIM Integrated Products, www.maxim-ic.com.

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